CS/B.TECH (EIE-New)/SEM-4/EI-402/2012

2012

MICROPROCESSOR & COMPUTER ARCHITECTURE

Time Allotted : 3 Hours Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Question)

1. Choose the correct alternatives for any *ten* of the following: 10 x 1 = 10

i) Whenever the PUSH instruction is executed in case of 8085 CPU, the stack pointer is

a) decremented by 1 b) decremented by 2

c) incremented by 1 d) incremented by 2.

ii) A single instruction to clear the lower four bits of the accumulator in 8085 microprocessor is

a) XRI OFH b) ANI FOH

c) ANI OFH d) XRI FOH

iii) Machine cycle in "CALL" instruction are

a) 6 b) 5

c) 4 d) 3.

iv) Address lines requires for 32 k-byte memory chip is

a) 13 b) 14

c) 15 d) 16.

v) The addressing mode used in the instruction LDAX B is

a) register b) immediate

c) register-indirect d) direct.

vi) Tri-state buffers are often used to make sure the unselected devices have their data outputs placed in the

a) Logic 1 state b) High-impedance state

c) Logic 0 state d) Input stage

vii) To perform Handshake I/O using 8255 PPI, which mode should be chosen?

a) Mode 0 b) Mode 1

c) Mode 2 d) Any of (a) and (b).

viii) For Opcode Fetch Machine Cycle the status signals of 8085 microprocessor is

a) $IO/\overline{M} = 0, S_1 = 0, S_0 = 1$

b) $IO/\overline{M} = 1, S_1 = 1, S_0 = 0$

c) $IO/\overline{M} = 0, S_1 = 1, S_0 = 0$

d) $IO/\overline{M} = 1, S_1 = 0, S_0 = 1$

ix) Which one of the following is the non-vectored interrupt of 8085 A microprocessor?

a) RST 7.5 b) EI

c) INTR d) TRAP.

x) The content of 'HL' register pair is 204A H. What will be the content of after executing the instruction DAD H?

a) 204A b) 4096

c) 4094 d) 2096.

xi) Whenever the Pop instruction is executed, the stack pointer is

a) decremented by 1 b) decremented by 2

b) incremented by 1 c) incremented by 2.

xii) When the instruction LHLD is executed, number of T-states required are

a) 10 b) 14

c) 13 d) 15.

xiii) SP register holds the

a) base address of stack

b) address of stack top

c) address of the instruction to be fetched

d) none of these.

xiv) Mode-2 o 8254 is

a) square wave generator

b) rate generator

c) software trigger strobe

d) hardware trigger strobe

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 x 5 = 15

2. a) What purpose does 'READY' signal serve in intel-8085 microprocessor?

b) Describe the bit assignment of the Flag Register in the 8085 microprocessor. 2+3

3. a) Define instruction cycle, machine cycle & T-state.

b) What will be the content of DE register pair at the end of the program?

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LXI SP, 2000H
LXI H, 1000H
DAD SP
XCHG
HLT.
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3+2

4. a) Differentiate memory mapped I/O and I/O Mapped I/O schemes.

b) What do you mean by Non-maskable (NMI) and Vectored interrupt? 3+2

5. a) What are the functions of program counter, stack pointer, ALE signal?

b) Write the control word format for I/O mode in 8255. 3+2

6. Draw the Timing diagram of MOV A, M instruction.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 x 15 = 45

7. a) The following block of data is stored in the memory locations from XX55H to XX5AH. Transfer the data to the locations XX80H to XX85H in the reverse order (e.g. the byte 22H should be stored at XX85H. and 37H at XX80H). Data (H) 22, A5, B2, 99, 7F, 37.

b) Write an assembly language program for packing & unpacking of any number.

c) What are interrupts? How many hardware interrupts are there? What are maskable & non-maskable interrupt? 5+5+5

8. a) Draw the timing diagram of the instruction STA 4000H and explain it.

b) A set of five 8-bit data is stored in five consecutive locations from XX00 to XX04. Write a program to arrange them in ascending order. (Choose XX as per your Kit). 10+5

9. a) Write accumulator bit pattern for RIM & SIM instruction.

b) Write a program to set PC4 and reset PC7 lines using BSR mode in 8255.

c) Design the I/O control word bit pattern to set port A in mode 2 and port B in mode 0 as input port. 3+4+6+2

10. a) Explain organization of a digital computer.

b) Differentiate between Harvard architecture and Von-Neumann architecture.

c) Describe the pipelining concept.

d) Differentiate between array processor and multiprocessor. 5+4+3+3

11. Write short notes on any *three* of the following: 3 x 5

a) Synchronous mode of data transfer

b) Interrupt service subroutine

c) handshaking mode of 8255

d) Designing I/O ports

e) Pipelining Hazards.

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