CS/B.TECH (CSE-New)/SEM-4/CS-403/2012

2012

COMPUTER ARCHITECTURE

Time Allotted : 3 Hours Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Question)

1. Choose the correct alternatives for the following: 10 x 1 = 10

   i) A pipeline stage

      a) is sequential circuit

      b) is combinational circuit

      c) consists of both sequential and combinational circuits

      d) none of these

   ii) utilization pattern of successive stages of a sunchronous pipeline can specified by

      a) truth table

      b) Excitation table

      c) Reservation table

      d) Periodic table

iii) SPARC stands for

a) Scalable Processor Architecture

b) Superscalar Processor A RISC Computer

c) Scalable Processor A RISC Computer

d) Scalable Pipeline Architecture

iv) Which of the following is **not** RISC architecture characteristic?

a) Simplified and unified format of code of instructions

b) No specialized register

c) No storage/storage instruction

d) Small register file

v) The time to access shared memory is same in which of the following shared memory multiprocessor models?

a) NUMA b) MIMD

c) SISD d) SIMD

vi) Which of the following architectures correspond to non-Neumann architecture?

a) MISD b) MIMD

c) SISD d) SIMD

vii) In absence of TLB, to access a physical memory location in a paged-memory system how many memory accesses are required?

a) 1 b) 2

c) 3 d) 4

viii) A direct mapped cache memory with n blocks is nothing but which of the following set associative cache memory organizations?

a) 0-way set associative

b) 1-way set associative

c) 2-way set associative

d) *n*-way set associative

ix) Probability is definitely an issue for which of the following architectures?

a) VLIW processor

b) Super Scalar processor

c) Super pipelined

d) None of these.

x) Which of the following is **not** the cause of possible data hazard?

a) RAR b) RAW

c) WAR d) WAW.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 x 5 = 15

2. "Instruction execution throughput increases in proportion with the number of pipeline stages". Is it true? Justify your statement.

3. What are multiprocessor, multi-computer and multi-core systems? Compare CISC and RISC computer architectures.

4. Describe Flynn's classification of computer architecture.

5. How is a block chosen for replacement in set-associative cache to resolve a cache miss?

6. How does principle of locality help in memory hierarchy design?

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 x 15 = 45

7. a) What is the difference between Computer Organization and Computer Architecture?

   b) Why does the equation to calculate the CPU-time of a program often expressed in terms of average CPI of that processor?

   c) A 30% enhancement in speedup for a component of the processor has been proposed for a new architecture. If the enhancement is usable only for 50% for the time, what is fraction of the time must enhancement be used to achieve an overall speedup of 10?

   d) What are the different approaches taken by pipeline processor to handle branch operations? Briefly illustrate any two approaches. 3 + 2 + 5 + 5

8. a) What are the major hurdles to achieve this ideal speed-up?

   b) Discuss data hazard briefly.

   c) Discuss briefly two approaches to handle branch hazards.

   d) Consider a 4-stage pipeline that consists of Instruction Fetch(IF), Instruction Decode(ID), Execution(Ex) and Write Back(WB) stages. The time taken by these stages are $50ns$, $60\,ns$, $110\,ns$ and $80\,ns$ respectively. The pipeline registers are required after every pipeline stages, and each of these registers comsumes 10 ns delay. What is the speedup of the pipeline under ideal conditions compare to the corresponding non-piplelined implementation? $2 + 5 + 4 + 4$

9. a) What do you mean by multiple issue processor?

   b) Briefly describe the VLIW processor architecture.

   c) What are the differences between superscalar processor and VLIW processor?

   d) Suppose your program consists of 2500 instructions. The proportion of different kinds of instructions in the program is as follows:

   Data transfer instruction 50%, architecture instruction 30% and branching related instructions 20%. The cycles consumed by these types of instructions are $2, 5$ and 10 respectively. What will be the execution time for a 4 GHz processor to execute your program? $2 + 5 + 3 + 5$

10. a) Discuss briefly MIMD architecture.

b) What is the significance of interconnection network in multiprocessor architecture?

c) An 8 kB 4-way set associative write back cache is organized as multiple blocks, each of 32 byte size. Assume that the processor generates 36 bits addresses. Calculate the total size of memory required by cache controller to store the tags for cache?

d) What are the approaches to improve miss penalty?

e) A CPU generates 32-bit virtual addresses. The page size is 4 kB. The processor has a TLB which can hold a total of 256 page table entries. The TLB is 8-way set associative. Calculate the TLB page size.

3 + 3 + 3 + 3 + 3

11. Write short notes on any *three* of the following: 3 x 5

a) Vector stride

b) Non von Neumann architecture characteristics

c) Cache coherence problem and its solution

d) Cluster Computer

e) Amdahl's law and its significance.

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