CS/B.TECH/EIE(New)/SEM-6/EI-603/2013

2013

ADVANCED MICROPROCESSORS AND MICROCONTROLLER

Time Allotted : 3 Hours Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Question)

1. Choose the correct alternatives for the following: 10 x 1 = 10

   i) What are the values present in CS and IP after resetting the 8086 microprocessor?

      a) Both contain 0000_H

      b) CS = 1000_H and IP = 0000_H

      c) CS = $FFFF_H$ and IP = 1000_H

      d) CS = $FFFF_H$ and IP = 0000_H

   ii) Which register is used to hold the address of the I/O device when I/O instructions are executed in the 8086 microprocessor?

      a) AX b) BX

      c) CX d) DX

iii) Pipelining improves CPU performance due to

a) reduced memory access time

b) increased clock speed

c) the introduction of parallelism

d) additional functional units.

iv) In 8086 microprocessor, which of the following has the highest priority among all type interrupts?

a) NMI b) Divide-by-0

c) Type 225 d) INTR.

v) In 8255 PPI, under the I/O mode of operation, which mode will have three I/O lines are available at Port C?

a) Mode 0 b) Mode 1

c) Mode 2 d) None of these.

vi) From which address the 8086 starts execution after reset?

a) 00000H b) 03*FF*0H

c) *EEEEF*H d) *FFFF*0H.

vii) Maximum I/O addressing capacity of 8086 is

a) 64 k b) 32 k

c) 128 k d) 256 k.

viii) Direction flag is used for

a) arithmetic operation b) transfer operation

c) string operation d) logical operation.

ix) $\overline{BHE}$ signal is used to select

a) higher order data bus

b) lower order data bus

c) lower order address bus

d) higher order address bus.

x) For isolated I/O we used separate control signal for

a) $\overline{IORC}$ operation

b) $\overline{IOWC}$ operation

c) $\overline{IORC}$ and $\overline{IOWC}$ operation

d) none of these.

xi) Two key lock out is used to prevent two key from being recognized

a) if pressed simultaneously

b) if pressed not simultaneously

c) both (a) & (b)

d) none of these.

xii) In 'JT NEXT' instruction of 8051 microcontroller which register is checked to see if it is zero?

a) A b) B

c) R1 d) R2.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 x 5 = 15

2. a) State the difference between 8086 and 8088 microprocessor.

b) Explain the physical address formation in 8086. 3 + 2

3. Explain the concept of segmented memory. What is its advantage?

4. Describe the different addressing modes of 8086.

5. a) Explain the different types of modes those are used in 8237 controller.

   b) Describe the function of different bits of command register. 2 + 3

6. Explain the memory organization of 8051 microcontroller.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 x 15 = 45

7. a) Draw and explain the functional block diagram of 8259A.

   b) Describe the priority scheme & EOI scheme of 8259.

   c) Write down the format of ICW1 & ICW2 of 8259.

   5 + 5 + 5

8. Write short notes on any *three* of the following: 3 x 5

   a) Clock generator 8284A

   b) BIU & EU

   c) Odd and even bank memory organizations of 8086

   d) DMA controller

   e) Bus controller 8288.

9. a) What do you mean by USART?

   b) Why USART is used?

c) Design the hardware interface circuit for interfacing 8251 with 8086. Set the 8251 in asynchronous mode as a transmitter and transmitter and receiver with even parity enabled, 2 stop bits, 8-bit character length, frequency is 160 kH and baud rate 10 K. Write an ALP to

i) Transmit 100 bytes of data string stored from 2000 : 3000H.

ii) Receive 100 bytes of data string and store it from 3000 : 4000H. 2 + 3 + (5 + 5)

10. a) Draw and discuss in brief the internal architecture of Intel 8051.

b) Describe different sources of interrupt in 8051.

c) Describe the functions of different bits of PSW register.

d) How many addressing modes are supported by 8051? State them with example. 6 + 3 + 3 + 3

11. Write short notes on any *three* of the following: 3 x 5

a) DMA operation

b) 8284 clock generator

c) Addressing modes of 8051 microcontroller

d) Interrupt operation of 8259 PIC in an 8086 system

e) 100 ms DELAY subroutine using 8086 microprocessor that runs at 10 MHz.